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10/799,139	03/12/2004	Christopher P. Duff	10040178-1	7920

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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,139	DUFF ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-53) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, *"Voutilainen does not recite the display of a representation of data samples of an analog signal".*

The examiner agrees. However, a new ground of rejection has been issued.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims (1-13, 16-17, 22-31, 34-35, 39-47, 50) are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong et al (hereinafter Jeong) (US Patent 6,229,859 B1) in view of Kirisawa. (US Patent 5,847,619)

Re claim 1, Jeong discloses a method for displaying digital interface symbol information from at least one analog signal, the digital interface symbol information including encoded symbols and decoded information, the method comprising: capturing a set of data samples of the at least one analog signal at a frequency higher than the switching rate of the at least one analog signal (See fig. 1: 106, col. 3, lines 47-62); converting the set of data samples into at least one serial bit stream using a clock (See fig. 6: 610 & fig. 8: 812 & col. 5, lines 32-34, 65 – col. 6, line 11. The data selector uses the data selection position from the data select controller to select a received data stream from the current over-sampled data stream.); searching the at least one serial bit stream for one or more sync symbols (See fig. 10: 1008 & col. 7, lines 41-43); identifying the encoded symbols in the at least one serial bit stream using the sync symbols (See col. 7, lines 50-55. One skilled in the art would know that once the sync symbols have been identified, the encoded symbols comprising the stream of data can easily be identified also.); and displaying at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion. (See col. 4, lines 5-10)

Although the reference of Jeong does teach displaying the received data graphically (See col. 4, lines 3-11), it fails to specifically disclose displaying at least

some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion.

However, Kirisawa does. (See figs. 1 & 3 & col. 1, lines 30-34, col. 3, lines 25-45, col. 4, lines 57-63) Kirisawa discloses a system a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator.

Taking the combined teachings of Jeong and Kirisawa as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Jeong, in the manner as claimed and as taught by Kirisawa, for the benefit of analyzing the phase modulated signal.

Re claim 2, the combination of Jeong and Kirisawa further discloses decoding the encoded symbols into the decoded information. (In Jeong, see fig. 1: 102 & 112)

Re claim 3, the combination of Jeong and Kirisawa further discloses that, wherein the frequency of the capturing step is at least eight times as high as the switching rate of the at least one analog signal. (In Jeong, see col. 5, lines 4-9)

Re claim 4, the combination of Jeong and Kirisawa further discloses recovering the clock from the at least one analog signal, the clock being an electronic signal. (In Jeong, see col. 5, lines 32-34)

Re claim 5, the combination of Jeong and Kirisawa further discloses that, wherein the recovering step is accomplished by way of an analog hardware phase-locked loop (PLL). (In Jeong, see col. 8, lines 55-64)

Re claim 6, the combination of Jeong and Kirisawa further discloses that, wherein the recovering step is accomplished by way of a digital hardware PLL. (In Jeong, see col. 5, lines 32-34)

Re claim 7, the combination of Jeong and Kirisawa further discloses recovering the clock from the set of data samples, the clock being a list of locations in time relative to the set of data samples. (In Jeong, see fig. 8: 806 & col. 5, lines 32-34)

Re claim 8, the combination of Jeong and Kirisawa further discloses that, wherein the recovering step is accomplished by a software PLL. (In Jeong, see col. 5, lines 32-34)

Re claim 9, the combination of Jeong and Kirisawa further discloses that, wherein the digital interface symbol information displayed by the displaying step are encoded symbols. (In Jeong, see col. 4, lines 5-10)

Re claim 10, the combination of Jeong and Kirisawa further discloses that, wherein the digital interface symbol information displayed by the displaying step is

decoded information. (In Jeong, see col. 4, lines 5-10)

Re claim 11, the combination of Jeong and Kirisawa further discloses that, wherein the encoded symbols comprise 10-bit symbols of an 8b/10b encoded interface. (In Jeong, see col. 3, lines 29-31)

Re claim 12, the combination of Jeong and Kirisawa further discloses that, wherein the decoded information comprises 8-bit data values and command codes of an 8b/10b encoded interface. (In Jeong, see col. 3, lines 29-31)

Re claim 13, the combination of Jeong and Kirisawa further discloses searching the digital interface symbol information for pre-selected symbol information. (In Jeong, see col. 10, lines 5-7)

Re claim 16, the combination of Jeong and Kirisawa fails to teach that, wherein the displaying step also displays high-level interface information derived from the decoded symbols with the representation of the set of data samples of the at least one analog signal in a correlated fashion. (In Jeong, see col. 4, lines 5-10)
However, the reference of Kirisawa does teach a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator. One skilled in the art would have

founded obvious to place the analyzer of Kirisawa at the output of the decoder of Jeong, in order to analyze the signals.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Jeong, as modified by Kirisawa, for the benefit of analyzing the phase modulated signal.

Re claim 17, the combination of Jeong and Kirisawa further discloses searching the high-level interface information for pre-selected symbol information. (In Jeong, see col. 10, lines 5-7)

Re claim 21, the combination of Jeong and Kirisawa further discloses an electronic device employing the method of claim 1. (In Jeong, see fig. 1)

Claim 22 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 22. Therefore, claim 22 has been analyzed and rejected w/r to claim 1 above.

Claim 23 is a system claim corresponding to method claim 2. Hence, the steps performed in method claim 2 would have necessitated the elements in system claim 23. Therefore, claim 23 has been analyzed and rejected w/r to claim 2 above.

Claim 24 is a system claim corresponding to method claim 3. Hence, the steps performed in method claim 3 would have necessitated the elements in system claim 24. Therefore, claim 24 has been analyzed and rejected w/r to claim 3 above.

Claim 25 is a system claim corresponding to method claim 4. Hence, the steps performed in method claim 4 would have necessitated the elements in system claim 25. Therefore, claim 25 has been analyzed and rejected w/r to claim 4 above.

Claim 26 is a system claim corresponding to method claim 7. Hence, the steps performed in method claim 7 would have necessitated the elements in system claim 26. Therefore, claim 26 has been analyzed and rejected w/r to claim 7 above.

Claim 27 is a system claim corresponding to method claim 9. Hence, the steps performed in method claim 9 would have necessitated the elements in system claim 27. Therefore, claim 27 has been analyzed and rejected w/r to claim 9 above.

Claim 28 is a system claim corresponding to method claim 10. Hence, the steps performed in method claim 10 would have necessitated the elements in system claim 28. Therefore, claim 28 has been analyzed and rejected w/r to claim 10 above.

Claim 29 is a system claim corresponding to method claim 11. Hence, the steps performed in method claim 11 would have necessitated the elements in system claim 29. Therefore, claim 29 has been analyzed and rejected w/r to claim 11 above.

Claim 30 is a system claim corresponding to method claim 12. Hence, the steps performed in method claim 12 would have necessitated the elements in system claim 30. Therefore, claim 30 has been analyzed and rejected w/r to claim 12 above.

Claim 31 is a system claim corresponding to method claim 13. Hence, the steps performed in method claim 13 would have necessitated the elements in system claim 31. Therefore, claim 31 has been analyzed and rejected w/r to claim 13 above.

Claim 34 is a system claim corresponding to method claim 16. Hence, the steps performed in method claim 16 would have necessitated the elements in system claim 34. Therefore, claim 34 has been analyzed and rejected w/r to claim 16 above.

Claim 35 is a system claim corresponding to method claim 17. Hence, the steps performed in method claim 17 would have necessitated the elements in system claim 35. Therefore, claim 35 has been analyzed and rejected w/r to claim 17 above.

Claim 39 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 39. Therefore, claim 39 has been analyzed and rejected w/r to claim 1 above.

Claim 40 is a system claim corresponding to method claim 2. Hence, the steps performed in method claim 2 would have necessitated the elements in system claim 40. Therefore, claim 40 has been analyzed and rejected w/r to claim 2 above.

Claim 41 is a system claim corresponding to method claim 3. Hence, the steps performed in method claim 3 would have necessitated the elements in system claim 41. Therefore, claim 41 has been analyzed and rejected w/r to claim 3 above.

Claim 42 is a system claim corresponding to method claim 4. Hence, the steps performed in method claim 4 would have necessitated the elements in system claim 42. Therefore, claim 42 has been analyzed and rejected w/r to claim 4 above.

Claim 43 is a system claim corresponding to method claim 7. Hence, the steps performed in method claim 7 would have necessitated the elements in system claim 43. Therefore, claim 43 has been analyzed and rejected w/r to claim 7 above.

Claim 44 is a system claim corresponding to method claim 9. Hence, the steps performed in method claim 9 would have necessitated the elements in system claim 44. Therefore, claim 44 has been analyzed and rejected w/r to claim 9 above.

Claim 45 is a system claim corresponding to method claim 10. Hence, the steps performed in method claim 10 would have necessitated the elements in system claim 45. Therefore, claim 45 has been analyzed and rejected w/r to claim 10 above.

Claim 46 is a system claim corresponding to method claim 11. Hence, the steps performed in method claim 11 would have necessitated the elements in system claim 46. Therefore, claim 46 has been analyzed and rejected w/r to claim 11 above.

Claim 47 is a system claim corresponding to method claim 12. Hence, the steps performed in method claim 12 would have necessitated the elements in system claim 47. Therefore, claim 47 has been analyzed and rejected w/r to claim 12 above.

Claim 50 is a system claim corresponding to method claim 16. Hence, the steps performed in method claim 16 would have necessitated the elements in system claim 50. Therefore, claim 50 has been analyzed and rejected w/r to claim 16 above.

4. **Claims (14-15, 18-20, 32-33, 36-38, 48-49, 51-53) are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong et al (hereinafter Jeong) (US Patent 6,229,859 B1) and Kirisawa (US Patent 5,847,619), as applied to claim 1 above, and further in view of Sajdak et al. (hereinafter Sajdak) (US Patent 6,570,592 B1)**

Re claim 14, the combination of Jeong and Kirisawa fails to specifically disclose triggering storage of the set of data samples based upon matching all or part of pre-selected symbol information with the digital interface symbol information.

However, Sajdak does. (See col. 7, lines 23-30) Sajdak discloses a logic analyzer comprising of a signal processor and a display processor. The signal processor samples and digitizes logic signals from a device under test (DUT), compares the resulting sampled data to user-selected trigger conditions, and, when the sampled data match the trigger condition, stores user-selected portions of the sampled data in a display memory.

Taking the combined teachings of Jeong, Kirisawa, and Sajdak as a whole, it would have been obvious to one of ordinary skill in the art to have incorporated this step into the system of Jeong, as modified by Kirisawa, in the manner as claimed and as taught by Sajdak, for the benefit of selecting, from a variety of signals, a signal for display. (See col. 7, line 32)

Re claim 15, the combination of Jeong, Kirisawa, and Sajdak fails to disclose that wherein the triggering step also repositions the digital interface symbol information and

the representation of the set of data samples of the at least one analog signal to a specified point.

However, the reference of Kirisawa does teach a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator. One skilled in the art would have founded obvious to place the analyzer of Kirisawa at the output of the decoder of Jeong, in order to analyze the signals.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Jeong, as modified by Kirisawa and Sajdak, for the benefit of analyzing the phase modulated signal.

Re claim 18, the combination of Jeong, Kirisawa, and Sajdak further disclose that triggering storage of the set of data samples based upon matching all or part of pre-selected symbol information with the high-level interface information. (This claim has been analyzed and rejected w/r to claim 14 above.)

Re claim 19, the combination of Jeong, Kirisawa, and Sajdak fails to disclose that, wherein the triggering step also repositions the high-level interface information and the representation of the at least one analog signal to a specified point.

However, the reference of Kirisawa does teach a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator. One skilled in the art would have

founded obvious to place the analyzer of Kirisawa at the output of the decoder of Jeong, in order to analyze the signals.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Jeong, as modified by Kirisawa and Sajdak, for the benefit of analyzing the phase modulated signal.

Re claim 20, the combination of Jeong, Kirisawa, and Sajdak fails to disclose that, wherein the displaying step also displays at least one clock location with the representation of the set of data samples of the at least one analog signal in a correlated fashion.

However, the reference of Kirisawa does teach a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator. One skilled in the art would have founded obvious to place the analyzer of Kirisawa at the output of the decoder of Jeong, in order to analyze the signals.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Jeong, as modified by Kirisawa and Sajdak, for the benefit of analyzing the phase modulated signal.

Claim 32 is a system claim corresponding to method claim 14. Hence, the steps performed in method claim 14 would have necessitated the elements in system claim 32. Therefore, claim 32 has been analyzed and rejected w/r to claim 14 above.

Claim 33 is a system claim corresponding to method claim 15. Hence, the steps performed in method claim 15 would have necessitated the elements in system claim 33. Therefore, claim 33 has been analyzed and rejected w/r to claim 15 above.

Claim 36 is a system claim corresponding to method claim 18. Hence, the steps performed in method claim 18 would have necessitated the elements in system claim 36. Therefore, claim 36 has been analyzed and rejected w/r to claim 18 above.

Claim 37 is a system claim corresponding to method claim 19. Hence, the steps performed in method claim 19 would have necessitated the elements in system claim 37. Therefore, claim 37 has been analyzed and rejected w/r to claim 19 above.

Claim 38 is a system claim corresponding to method claim 20. Hence, the steps performed in method claim 20 would have necessitated the elements in system claim 38. Therefore, claim 38 has been analyzed and rejected w/r to claim 20 above.

Claim 48 is a system claim corresponding to method claims 13 & 14. Hence, the steps performed in method claims 13 & 14 would have necessitated the elements in system claim 48. Therefore, claim 48 has been analyzed and rejected w/r to claims 13 & 14 above.

Claim 49 is a system claim corresponding to method claim 15. Hence, the steps performed in method claim 15 would have necessitated the elements in system claim 49. Therefore, claim 49 has been analyzed and rejected w/r to claim 15 above.

Claim 51 is a system claim corresponding to method claim 18. Hence, the steps performed in method claim 18 would have necessitated the elements in system claim 51. Therefore, claim 51 has been analyzed and rejected w/r to claim 18 above.

Claim 52 is a system claim corresponding to method claim 19. Hence, the steps performed in method claim 19 would have necessitated the elements in system claim 52. Therefore, claim 52 has been analyzed and rejected w/r to claim 19 above.

Claim 53 is a system claim corresponding to method claim 20. Hence, the steps performed in method claim 20 would have necessitated the elements in system claim 53. Therefore, claim 53 has been analyzed and rejected w/r to claim 20 above.

5. Claims (1, 22, 39) are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong et al (hereinafter Jeong) (US Patent 6,229,859 B1) in view of Iida. (US Patent 7,236,513 B2)

Re claim 1, Jeong discloses a method for displaying digital interface symbol information from at least one analog signal, the digital interface symbol information including encoded symbols and decoded information, the method comprising: capturing

a set of data samples of the at least one analog signal at a frequency higher than the switching rate of the at least one analog signal (See fig. 1: 106, col. 3, lines 47-62); converting the set of data samples into at least one serial bit stream using a clock (See fig. 6: 610 & fig. 8: 812 & col. 5, lines 32-34, 65 – col. 6, line 11. The data selector uses the data selection position from the data select controller to select a received data stream from the current over-sampled data stream.); searching the at least one serial bit stream for one or more sync symbols (See fig. 10: 1008 & col. 7, lines 41-43); identifying the encoded symbols in the at least one serial bit stream using the sync symbols (See col. 7, lines 50-55. One skilled in the art would know that once the sync symbols have been identified, the encoded symbols comprising the stream of data can easily be identified also.); and displaying at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion. (See col. 4, lines 5-10)

Although the reference of Jeong does teach displaying the received data graphically (See col. 4, lines 3-11), it fails to specifically disclose displaying at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion.

However, Iida does. (See figs. 2A-N & col. 6, line 39—col. 7, line 12) Iida discloses displaying the IQ signal (data samples) modulated (correlated fashion) with a carrier signal.

Taking the combined teachings of Jeong and Iida as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the

system of Jeong, in the manner as claimed and as taught by Iida, for the benefit of analyzing the phase modulated signal.

Claim 22 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 22. Therefore, claim 22 has been analyzed and rejected w/r to claim 1 above.

Claim 39 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 39. Therefore, claim 39 has been analyzed and rejected w/r to claim 1 above.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. F./
Examiner, Art Unit 2611
March 28, 2008

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611